UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,884	04/21/2004	Bor-Min Tseng	TSM03-0763	5862

43859 7590 05/10/2006

SLATER & MATSIL, L.L.P.
17950 PRESTON ROAD, SUITE 1000
DALLAS, TX 75252

EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,884	TSENG, BOR-MIN	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *20-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9,12,14,15,18 and 19* is/are rejected.

7)☒ Claim(s) *5-8,10,11,13,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *042104*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-19 in the reply filed on April 6th, 2006 is acknowledged. The traversal is on the ground(s) that the claims of Group I and Group II are closely related such that examination of both groups would not pose an undue burden on the Examiner. This is not found persuasive because these inventions are distinct and have acquired a separate status in the art as shown by their different classification, therefore, the search are non-coextensive. Thus, restriction for examination purposes as indicated is proper. The requirement is still deemed proper and is therefore made FINAL.
2. Claims 20-30 withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected claims, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on April 6th, 2006.

Preliminary Amendment

3. The preliminary amendment filed on November 3rd, 2005 has been entered.

Oath/Declaration

4. The oath/declaration filed on April 21st, 2004 is acceptable.

Information Disclosure Statement

5. The Information Disclosure Statement filed on April 21st, 2004 has been considered.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

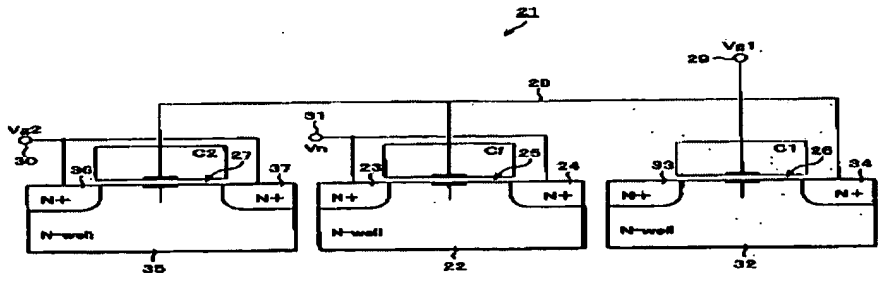
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 3, 9, 12, 14, 15, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Adan (U.S. Pub. 2003/0136992).

In re claim 1, **Adan** disclose a method of forming a semiconductor varactor device 21 having improved linearity comprising the steps of:

providing a semiconductor substrate (single silicon substrate) (page 4, paragraph [0055]); forming at least a first and a second differential varactor element on the semiconductor substrate, the forming of each of the differential varactor elements comprising the steps of forming first **36**, second **37** and third **24** N+ doped regions in an N well **35**, forming a first gate **C2** for controlling the first **36** and second **37** N+ doped regions and forming a second gate **Cf** for controlling the second **37** and third **24** N+ doped regions (pages 3-4, paragraphs [0051]-[0053] and FIG. 5);

FIG. 5

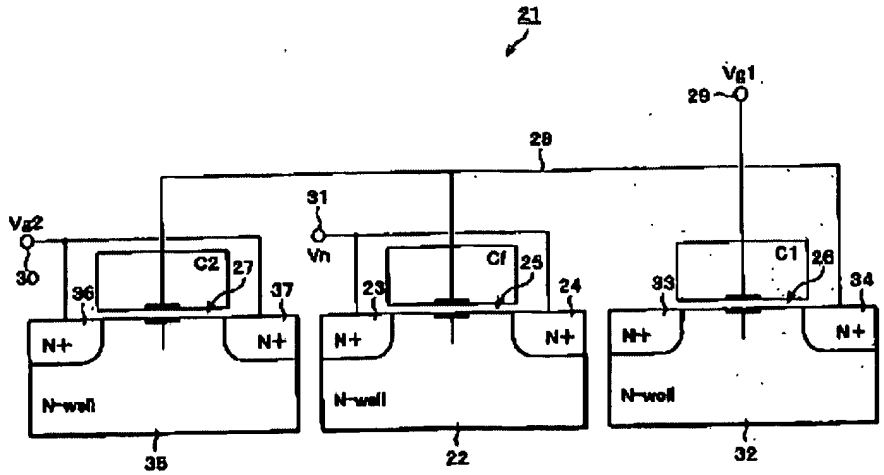


connecting the first **36**, second **37** and third **24** N+ doped regions of the first differential varactor element to receive power having a first voltage **Vg2**; and connecting the first **33**, second **34** and third N+ doped regions of the second differential varactor element to receive power having a second voltage **Vg1** different than the first voltage (page 4, paragraphs [0053]-[0055] and FIG. 5).

In re claim 3, as applied to claim 2 above, **Adan** discloses all claimed limitations including the limitation wherein the step of forming the first **C2** and second **Cf** gates comprises the step of forming a first N-type gate and forming a second N-type gate (page 3, paragraph [0052]).

In re claim 9, as applied to claim 1 above, **Adan** discloses all claimed limitations including the limitation connecting the first gate **C2** of the first and second differential varactor elements together at a first terminal **Vg2** and connecting the second gate **Cf** of the first and second differential varactor elements together at a second terminal **Vn** (page 4, paragraph [0055] and FIG. 5)

FIG. 5



In re claim 12, as applied to claim 9 above, **Adan** discloses all claimed limitations including the limitation connecting the first **Vg2** and second **Vg1** terminals to an oscillator circuit as a voltage controlled capacitor (page 6, paragraph [0084] and FIG. 5).

In re claim 14, as applied to claim 1 above, **Adan** discloses all claimed limitations including the limitation wherein the forming steps are according to a CMOS process (page 4, paragraph [0060]).

In re claim 15, as applied to claim 9 above, **Adan** discloses all claimed limitations including the limitation wherein first **C2** and second **Cf** gates are N-type gates (page 3, paragraph [0052]).

In re claim 18, as applied to claim 1 above, **Adan** discloses all claimed limitations including the limitation forming another differential varactor element on the semiconductor, the another differential varactor element comprising first, second and third P+ doped regions in a P well, a first gate for controlling the first and second P+ doped regions and a second gate for controlling said second and third P+ doped regions, and connecting said first, second and third P+ doped regions to receive power from the voltage source (FIG. 5).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 4, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adan (U.S. Pub. 2003/0136992) in view of Jasa et al. (U.S. Pub. 2005/0212609).

In re claim 2, as applied to claim 1 Paragraph 6 above, **Adan** discloses all claimed limitations including the limitation wherein the step of connecting the first **36**, second **37** and third **24** N+ doped regions of the first differential varactor comprises connecting to the voltage source **Vg2** (FIG. 5) but does not explicitly disclsoes wherein the step of connecting the first, second and third N+ doped regions of the second differential varactor comprises connecting to the voltage source through the first resistor.

Jasa, however, discloses a varactor pair having the step of connecting the first, second and third N+ doped regions of the common N Well of the second differential varactor comprises connecting to the voltage source V_{cp} through the first resistor **R3** (page 3, paragraphs [0028]-[0030] and FIG. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Adan and Jasa to enable the process of connecting the first, second and third N+ doped regions of the second differential varactor comprises connecting to the voltage source through the first resistor of Adan to be performed and furthermore to generate a differential oscillating waveform (col. 2, paragraph [0012], Jasa).

In re claim 4, as applied to claim 2 above, **Adan** discloses all claimed limitations including the limitation wherein the step of connecting the first **36**, second **37** and third **24** N+ doped regions of the first differential varactor comprises connecting to the voltage source **Vg2** (FIG. 5) but does not explicitly disclose connecting the regions to the voltage

source through another resistor, and such that the second differential varactor elements receive power from the voltage source through both of another and the first resistors.

Jasa, however, discloses a varactor pair having the step of connecting the first, second and third N+ doped regions of the common N Well of the second differential varactor comprises connecting to the voltage source $\mathbf{V_{cn}}$ through the another resistor **R2**, and such that the second differential varactor elements received power from the voltage source $\mathbf{V_{cn}}$ through both of another **R2** and the first **R1** resistors (page 3, paragraphs [0028]-[0030] and FIG. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Adan and Jasa to enable the process of connecting the regions to the voltage source through another resistor, and such that the second differential varactor elements receive power from the voltage source through both of another and the first resistors to be performed and furthermore to generate a differential oscillating waveform (col. 2, paragraph [0012], Jasa).

In re claim 19, as applied to claim 2 above, neither Adan nor Jasa disclsoes that the step of forming the first resistor from a polysilicon material. The reference, Ohkubo et al. (U.S. Pub. 2004/0188795), provided herein as evidence to show that the process of forming the first resistor from a polysilicon material is well-known to one of ordinary skill in the art at the time of the invention was made (page 2, paragraph [0015], Ohkubo).

Allowable Subject Matter

10. Claims 5-8, 10, 11, 13, 16, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in

independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede

BROOK KEBEDE
PRIMARY EXAMINER

K.N.
May 7, 2006